What is Claimed is:

1. A circuit for generating aligned clock and data signals, comprising:

a clock input;

a first circuit path receiving an external clock signal from said clock input, and generating an aligned clock signal; and

a second circuit path generating an aligned data signal;

wherein said first and second circuit paths comprise identical circuit components.

2. The circuit as claimed in claim 1, wherein said first and second circuit paths each comprises a D flip-flop and an output buffer.

3. The circuit as claimed in claim 2, further comprising a clock multiplication circuit for receiving said external clock signal and sending a multiplied clock signal to said D flip-flops in said first and second circuit paths.

4. The circuit as claimed in claim 3, wherein said clock multiplication circuit comprises a clock multiplier and an inverter.

5. A circuit for generating aligned clock and data signals, comprising:

a clock input;

an inverter receiving an external clock signal from said clock input and generating an inverted clock signal;

a first circuit path receiving said inverted clock signal from said inverter, and generating an aligned clock signal; and

a second circuit path generating an aligned data signal;

wherein said first and second circuit paths comprise identical circuit components.

6. The circuit as claimed in claim 5, wherein said first and second circuit paths each comprises a D flip-flop and an output buffer.

7. The circuit as claimed in claim 6, further comprising a clock multiplier receiving said external clock signal and sending a multiplied clock signal to said D flip-flop in said second circuit path, and an inverter receiving said multiplied clock signal and sending an inverted multiplied clock signal to said D flip-flop in said first circuit path.

8. A circuit for generating aligned clock and data signals, comprising:

a clock input;

an inverter receiving an external clock signal from said clock input and generating an inverted clock signal,

a first circuit path receiving said inverted clock signal from said inverter, and generating an aligned clock signal;

a second circuit path generating an aligned data strobe signal;

a third circuit path generating an aligned first data signal; and

a fourth circuit path generating an aligned second data signal;

wherein said first, second, third and fourth circuit paths comprise identical circuit components.

9. The circuit as claimed in claim 8, wherein said first, second, third and fourth circuit paths each comprises a D flip-flop and an output buffer.

10. The circuit as claimed in claim 9, further comprising a clock multiplication circuit receiving said external clock signal, sending a multiplied clock signal to said D flip-flops in said third and fourth circuit paths, and sending an inverted multiplied clock

signal to said D flip-flops in said first and second circuit paths.

11. The circuit as claimed in claim 10, said clock multiplication circuit comprising a clock multiplier receiving said external clock signal and sending a multiplied clock signal to said D flip-flops in said third and fourth circuit paths, an inverter receiving said multiplied clock signal and sending an inverted multiplied clock signal to said D flip-flop in said first circuit path, and an inverter receiving said multiplied clock signal and sending an inverted multiplied clock signal to said D flip-flop in said second circuit path.